Virtio-SCIF: Enabling Xeon Phi capabilities on Virtual Machines

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Motivation

- **Coprocessor Virtualization**
- Use Case: *Intel Xeon Phi*
- Currently, it is not possible for many VMs to share a single Xeon Phi
- Full coprocessor virtualization involves complex implementation details
- Current "alternatives":
  - Direct device assignment to a single VM (via PCIe passthrough)
  - TCP/IP through Xeon Phi virtual network device

Xeon Phi Modes of Execution

i) **Native Mode**: applications are executed in a coprocessor-only way

ii) **Offload Mode**: the coprocessor can be used by the host as an accelerator by offloading certain workloads

iii) **Symmetric Mode**: allows both the host CPUs and the coprocessors to be involved in the execution of MPI processes in a symmetric way

Symmetric Mode

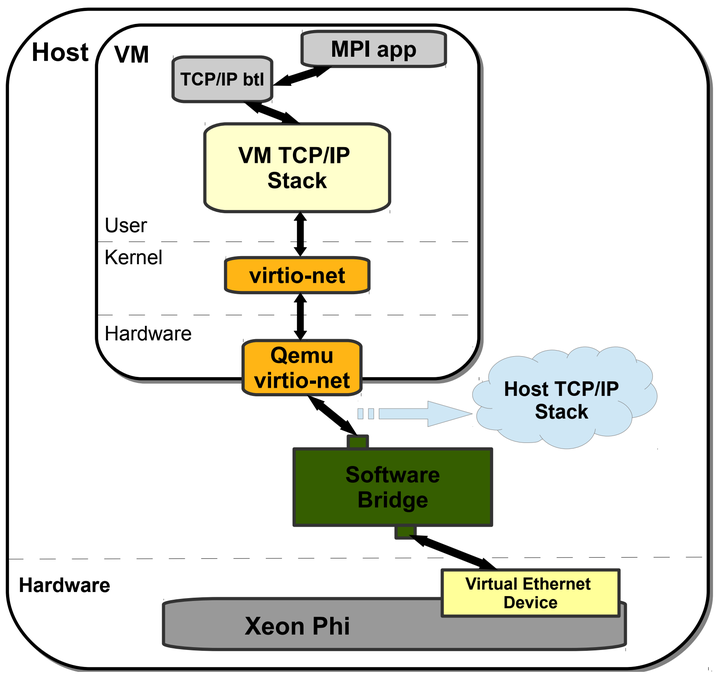
SCIF: Symmetric Communication Interface

- Transport layer between Host and Xeon Phi card(s)
- Directly exposes the DMA capabilities of Xeon Phi
- Uniform API across PCIe
- Socket-like API
- Provides both one-way and two-way communication semantics
- Many MPI implementations currently support SCIF transport

Virtio-SCIF

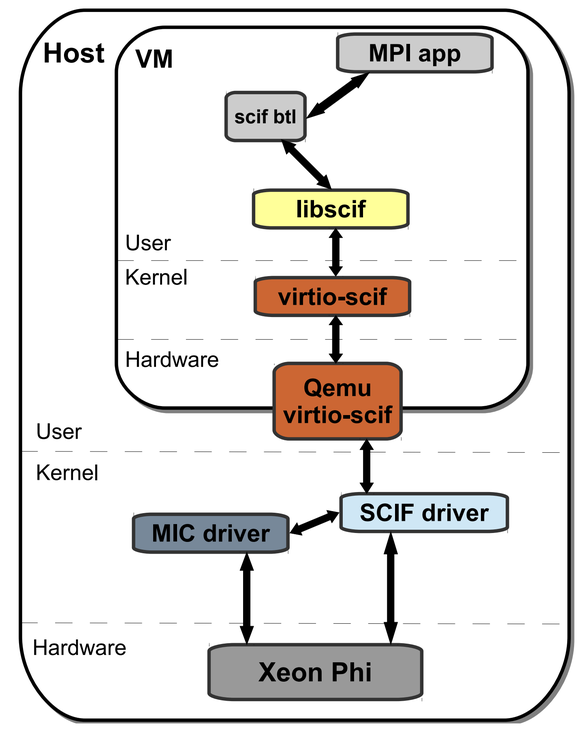
- *Main Idea*: virtualizing a generic transport between host and coprocessor devices
- Targeting cloud environments hosting HPC applications
- *Proof of concept*:
  - Virtualizing SCIF transport layer providing VMs with Xeon Phi capabilities
  - Virtual device implementation using Virtio specification
  - VMs can execute MPI over SCIF transparently with lower latency
- *Vision*:
  - Unify different coprocessors/accelerators transports
  - Provide coprocessor sharing to VMs by cloud providers
  - VMs can benefit and accelerate data-parallel applications

Current I/O Path



- Intel provides an implementation of a virtual ethernet device in its software stack
- VMs can execute MPI over TCP/IP
- Involves unnecessary TCP/IP traversal both in the VM as well as in the host

Proposed I/O Path



- Communication with SCIF semantics
- No application (source or binary) modification needed
- Avoids costly TCP/IP processing
- Low-latency, high-throughput communication
- Better scalability across multiple VMs sharing the same coprocessor card

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