Dionisios N. Pnevmatikatos

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April 2nd, 2020

Education

B.S.   January 1989, *University of Crete, Department of* Computer Science

M.Sc.   May 1991, *University of Wisconsin–Madison,* Computer Sciences Department

Ph.D.   December 1995, *University of Wisconsin–Madison*, Computer Sciences Department

Research Interests

My research interests are in the broader area of Computer Architecture, while my current focus is on using reconfigurable computing to create highly efficient, accelerated, heterogeneous parallel/rack-scale systems. I have also worked on Reliable System Design, Networking Hardware and Network Processors, Application Acceleration, Custom and Application-Specific Architectures, and Hardware Acceleration of Bioinformatics Algorithms.

Employment

September 2019 – : Professor, School of Electronic and Computer Engineering, National Technical University of Athens

February 1997–December 2019: FORTH-ICS (*02/97–08/00*: *Researcher, 09/00-12/19*: *Research Associate)*

August 2000– September 2019: Professor, Electronic and Computer Engineering Department, Technical University of Crete, (Assistant Professor until September 2002, Associate Professor until November 2009). Director, MHL Laboratory

September 2007 - August 2009: Chair, Electronic and Computer Engineering Department

February 2015-January 2016: Visiting Professor, PARSA Laboratory, EPFL

Awards- Distinctions

ACM/SIGDA Technical Committee on FPGAs (TCFPGA) Hall of Fame 2020 Committee member (http://hof.tcfpga.org/)

"Significant paper" (or test-of-time) award, FPL conference. Paper [C16] was selected among the 27 papers with the most impact from the first 25 years of the FPL conference (number of citations and citations over time)

HiPEAC Award for the paper "Formic: Cost-efficient and Scalable Prototyping of Manycore Architectures», Spyros Lyberis, George Kalokerinos, Michalis Lygerakis, Vassilis Papaefstathiou, Dimitris Tsaliagkos, Manolis Katevenis, Dionisios Pnevmatikatos, Dimitris Nikolopoulos, published at Field-Programmable Custom Computing Machines, 2012, https://www.hipeac.net/research/paper-awards/2012/

Funding/Project Participation

Since 2010, I have secured grants for a total budget of almost 2.4M€ (90% EU research projects), and I coordinated FASTER, a 3.7M€ FP7 ICT project. I am currently the Coordinator for the EDRA H2020 project. The current size of my research team is two post-doc staff, one staff engineer, two PhD, three MSc and several undergraduate students. In more detail, my funding record is the following:

- EDRA, H2020 FET-HPC CSA, *Project Coordinator* for TSI/TUC, May 2019, one year project to capitalize on the results of EXTRA, budget 100K€

- dRedBox, H2020, *Project Technical Coordinator* and Scientific Coordinator FORTH/ICS (CARV

Laboratory), 2016-2018, budget 532K€

- EXTRA, H2020/FET-HPC, Scientific Coordinator for TSI/TUC, Sept 2015-Aug2018, budget 420K€
- AXIOM, H2020, Scientific Coordinator for FORTH/ICS (CARV Laboratory), Feb 2015-Jan 2018, budget 320K€
- FASTER – Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration, ICT STREP, *Coordinator*, Sept 2011-Nov 2014, budget 480K€, total budget 3.7M€
- DeSyRe – on-Demand System Reliability, ICT STREP, Scientific Coordinator FORTH/ICS (CARV Laboratory), Oct 2011-Jan 2015, budget 360K€
- mCluster: Development of Standard Integrated Infrastructure for the resolution of complex computational problems, Funding Source: General Secretariat for Research and Technology, Budget: €99.000,00, Duration: Apr. 2014 – Jul. 2015
- MERIT: "An Integrated RFID-based System for Securing And Speeding-Up Marine Transportations", Funding Source: National Strategic Reference Framework (NSRF 2007 - 2013), Sectoral Operational Programmes, Competitiveness and Entrepreneurship, Budget: €66.904,35, Duration: May 2011 – Oct. 2014
- PI at the ECE School Practical Training Program 2006-2015
- Encore – ENabling technologies for a programmable many-CORE, ICT STREP (member)
- SARC – Scalable computer ARChitecture, ICT Integrated Project aiming to develop a scalable integrated architecture applicable to a wide range of applications (member)
- HiPEAC– European Network of Excellence on High Performance and Embedded Architecture and Compilation, ICT Network of Excellence, Member of the Interconnects and Reconfigurable Computing Clusters (member)
- VPLANET: Advanced Verification and Emulation Platform, GSRT, Scientific Coordinator, 2006-2008
- EASY/HIPERLAN: Advanced Pipelining and Implementation of a HIPERLAN Wireless Modem, 2003-2004
- PRO3 – Architecture, Design and Implementation of the I/O Subsystem of a Network Processor, 2000-2002
- PENED 1999: PLATO: A Development Platform for Protocol Boosting in ATM networks (GSRT, graded 9.9/10)
- ASSICOM – Design and Implementation of the ATLAS I ATM single chip switch (member)
- SPEAR-II – Superscalar Network Processor Architecture (member)

Teaching
Since September 1997 I have taught many courses in Computer Architecture and Digital Design, both at undergraduate and graduate levels, and in the Department of Computer Science of the University of Crete and in the Electronic and Computer Engineering Department of the Technical University of Crete. The nominal load is two undergraduate and one graduate course per academic year, and the undergraduate courses I taught are:
- Digital Design
- Advanced Digital Design
- Digital Computers (Assembly)
- Computer Organization
- Computer Architecture
- Advanced Computer Architecture

The graduate courses are:
- Parallel Computer Architecture (University of Crete)
- Advanced Processor Architectures
- Special Topics in Computing System Design
- Designing Application Specific Architectures
- Network Processor Architecture

I designed the undergraduate courses Advanced Digital Design, Advanced Computer Architecture, and all the graduate courses I teach, and I significantly revamped the undergraduate courses Digital Computers and Computer Architecture.

Together with Professors D. Serpanos and G Stamoulis, I translated the 3rd edition of the "Computer Architecture – A Quantitative Approach" by J. L. Hennessy, D. A. Patterson, a reference book in Computer Architecture.

Student Advising

In the Technical University of Crete since August 2000 I have supervised more than 47 undergraduate diploma and 10 Master thesis, and I have graduated 2 Ph.D. students, and actively co-advised another three (I. Sourdis, G. Passas, N. Chrysos).

Ph.D. Graduated:

George Kornaros, Dec 2013

Ioannis Mavroidis Dec. 2011

Georgios Passas (Co-advisor), Feb 2012

Ioannis Sourdis (Co-advisor), Dec 2007

PhD. Examination Committees:

"Opponent", Department of Electrical Engineering, Linköping University, Sweden, 2004 (Dr. Ulf Nordqvist).

TU-Delft, December 2007 (I. Sourdis), May 2011 (D. Theodoropoulos), June 2011 (Daniele Ludovici), June 2011 (T. Marconi), June 2015 (H. Mushtaq)

Ghent University: Fatma Abouelella

University of Crete: G. Passas, V. Papaefstathiou, S. Lyberis, N. Chrysos, S. Kavvadias

Democritus University of Thrace: K. Siozios

National Technical University of Athens: D. Diamantopoulos

University of Thessaly: M. Koziri, D. Mountas, G. Giannakas

University of Patras: G. Keramidas

Technical University of Crete: Karkazis Panagiotis, Nikitakis Antonis, Sotiriadis Evripidis, Koutroulis Eftichios, Chatzakis Ioannis

University of Uppsala: Vassilis Spilopoulos, Konstantinos Koukos

Departmental Duties, Committees, etc.

- Chair, Electronic and Computer Engineering Department, September 2007-August 2009
- Scientific Coordinator for the Network Operation Center of the Technical University of Crete, October 2002 – March 2006
- Scientific Coordinator of the Departmental Practical Training Program, 2006-now.
- Various employee selection and employee promotion evaluation committees

Citations

On Mar. 25th, 2019, Google Scholar reported 2703 citations, an h-index of 27, and an i10 index of 51, and Scopus reported 1185 citations and an h-index of 17. On Oct. 15th, 2018 Google Scholar reported 2595 citations, an h-index of 25, and an i10 index of 51, and Scopus reported 954 citations and an h-index of 17. Historical citation data to my works (*with all self-citations by me or by co-authors as reported by Google Scholar*) were (citations/h-index): ~820/13 on February 2009, ~1250/17 on April 2011, ~1464/18 on March 2013, and ~1680/20 citations on Jan 2014, 2167/23 on Sept 2016.

Professional Service

Expert Reviewer:

- ECSEL proposal evaluator, 2017
- Corallia Microelectronics Cluster, 2010-2014
- Artemis/ECSEL June 2013, June 2014, Nov 2014, June 2015, December 2015, June 2016

- Eurostars 2009-now
- Cyprus NSF (2009)
- Canadian National Research Foundation (NSERC), 2015, 2016

Program Co-Chair:
- 21st International Conference on Field Programmable Logic and Applications (FPL), 2011
- HIPEAC Workshop on Reconfigurable Computing (WRC), 2012

Program Chair:
- International Conference on Embedded Computer Systems: Architectures, Modelling, and Simulation (SAMOS) 2018
- Design and Test Europe (DATE) Architecture and Microarchitecture Track, 2009, 2010

Program Co-Chair:
- Design and Test Europe (DATE) Architecture and Microarchitecture Track, 2007, 2008
- Topic co-chair, Multicore and Manycore Programming at Euro-Par 2012

General Chair:
- International Conference on Embedded Computer Systems: Architectures, Modelling, and Simulation (SAMOS) 2019

General Co-Chair:
- Panhellenic Conference on Informatics (PCI) 2008
- International Workshop on Rapid System Prototyping (RSP) 2007
- HIPEAC Workshop on Reconfigurable Computing (WRC), 2013

Conference Technical Committee Member:
- International Symposium on Microarchitecture (MICRO), 2011
- Design and Test Europe (DATE), Architecture and Microarchitecture Track, 2006, 2011-2016
- International Conference on Field Programmable Logic and Applications (FPL), 2007-2016
- International Conference on Embedded Computer Systems: Architectures, Modelling, and Simulation (IC-SAMOS) 2006-2016
- International Workshop on Rapid System Prototyping (RSP) 2006-2012
- International Conference on Supercomputing (ICS) 2006, 2007, 2012
- IEEE International Parallel & Distributed Processing Symposium (IPDPS) 2007
- International Conference on Computer Design (ICCD) 2007-2014
- International Conference on Parallel Processing (ICPP), Architecture Track 2002, 2009, 2010
- Computing Frontiers 2007
- Reconfig 2012-2015
- RAW 2014, 2015, 2016
- IEEE International Symposium on Circuits and Systems (ISCAS) 2007
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-Soc) 2008-2010, 2014
- International Symposium on Signal Processing and Information Technology (ISSPIT) 2006
- IEEE International ASIC/SOC Conference (ASIC) 2000-2002
- Panhellenic Conference on Informatics (PCI) 2005, 2008, 2009

Workshop Technical Committee Member:
- HIPEAC-RC (Reconfigurable Computing) 2007, 2008, 2009, 2014-16
- HIPEAC- Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC), 2007-2009

Journal Reviewer:
- IEEE Micro
- ACM Transactions on Architecture and Code Optimization (TACO, ``distinguished reviewer'')

- ACM Transactions on Embedded Systems (TECS)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on VLSI Systems (TVLSI)
- IEEE Transactions on Networking (TON)
- International Journal on Parallel Processing - Springer
- International Journal on Reconfigurable Computing - Hindawi
- Journal of Parallel and Distributed Computing - Elsevier
- Journal of Systems Architecture
- Computer Architecture Letters
- Computer Networks, The International Journal of Computer and Telecommunications Networking (COMNET)
- IET Computers & Digital Techniques
- Electronics and Telecommunications Research Institute Journal (ETRI), South Korea.

Conference Reviewer:
- International Symposium on Computer Architecture (ISCA) 1993, 1995, 1998
- Architectural Support for Programming Languages and Operating Systems (ASPLOS) 1994
- IEEE/ACM International Symposium on Microarchitecture (MICRO) 2001
- IEEE Symposium on High-Performance Computer Architecture (HPCA) 1995, 2008
- International Conference on Computer Design (ICCD) 1997-1998
- International Conference on Parallel Architectures & Compilation Techniques (PACT) 1999, 2001
- International Conference on Supercomputing (ICS) 2000, 2001, 2007
- IEEE International Parallel & Distributed Processing Symposium (IPDPS) 2007
- IEEE International on ASIC/SOC Conference (ASIC) 2000-2002
- The 8th Workshop on Hot Topics in Operating Systems (HotOS-VIII) 2001
- IEEE International Symposium on Circuits and Systems (ISCAS) 2007
- International Conference on New Technologies, Mobility and Security (NTMS) 2007
- 9th International World Wide Web Conference (WWW9) 1999
- International Workshop on Agents and Peer-to-Peer Computing (AP2PC) 2002
- Pan-Hellenic Informatics Conference (PCI) 2000-2001
- SIGDA PhD Forum at Design Automation Conference 2002

Advisory Board Member:

Europar Conference 2012, http://www.fim.uni-passau.de/Europar_ab_liste.html

Guest Editor:

ACM Transactions on Embedded Computing Systems (TECS), Special Issue on Rapid System Prototyping, Volume 7, Issue 4 (July 2008).

Invited Talks

Keynote, "Reconfigurable Acceleration for HPC and Data-Center Application Acceleration", EuroExaScale: Towards European Exascale HPC Worksop", co-located with the HiPEAC 2019 Conference, in Valencia, January 2019

Keynote, 5th DEPCP Friday Workshop of DATE 2013

University of Ioannina, Computer Sciences Department, June 1998, ``Computer Architecture around the Turn of the Century''

Publications

Books & Book Chapters:

[B1] Sotiris Ioannidis, Athanasios Papathanasiou, Gregorios Maglis, Evangelos Markatos, Dionisios Pnevmatikatos, and Julia Sevaslidou, ``On Using Reliable Network RAM in Networks of Workstations'', Cluster Computing, pp. 109-121, Chapter 10, 2001, ISBN 1-59033-113-3, Nova Science Publishers, USA.

[B2] George Kornaros, Ioannis Papaeystathiou, and Dionisios Pnevmatikatos, ``Real-time Monitoring and Diagnostic Services for Networks-on-Chip'', Chanter 9, Networks-on-Chips: Theory and Practice, In Press, Publisher: Taylor & Francis Group LLC - CRC Press, Editors: Fayez Gebali, Haytham Elmiligi, and M.Watheq El-Kharashi, 2009.

[B3] Koen De Bosschere, Wayne Luk, Xavier Martorell, Nacho Navarro, Mike O'Boyle, Dionisios Pnevmatikatos, Alex Ramirez, Pascal Sainrat, André Seznec, Per Stenström, Olivier Temam, ``High-Performance Embedded Architecture and Compilation Roadmap'', *Transactions on High-Performance Embedded Architectures and Compilers*. Springer-Verlag. Vol. 1 (1). 2007. pp. 5-29.

[B4] «Embedded Systems Design with FPGAs», Athanas, Peter; Pnevmatikatos, Dionisios; Sklavos, Nicolas (Eds.), Springer, ISBN 978-1-4614-1362-2, 2012

Journal Publications

[J1] Jeffrey D. Gee, Mark D. Hill, Dionisios N. Pnevmatikatos, and Alan J. Smith, ``Cache Performance of the SPEC92 Benchmark Suite,'' IEEE Micro, August 1993.

[J2] Sotiris Ioannidis, Athanasios Papathanasiou, Gregorios Maglis, Evangelos Markatos, Dionisios Pnevmatikatos, and Julia Sevaslidou, ``On Using Reliable Network RAM in Networks of Workstations'', *Parallel and Distributed Computing Practices (PDCP)*, Special Issue on High Performance Computing Clusters, Vol. 2, No. 5, Nova Science Publishers, USA, May 1999.

[J3] Georgios Kornaros, Dionisios Pnevmatikatos, Panagiota Vatsolaki, Georgios Kalokerinos, Chara Xanthaki, Dimitrios Mavroidis, Dimitrios Serpanos, and Manolis Katevenis, ``Implementation of ATLAS I: a Single-Chip ATM Switch with Backpressure'', IEEE *Micro*, vol. 19, n. 1, pp. 30-41, February 1999.

[J4] Dionisios Pnevmatikatos, Evangelos Markatos, Gregory Maglis, and Sotiris Ioannidis, ``On Using Network RAM as a non-volatile Buffer'', *Cluster Computing: The Journal on Networks, Software and Applications*, Special Issue on I/O in Shared-Storage Clusters, (4), pp. 295-303, Baltzer Science Publishers, 1999.

[J5] Evangelos Markatos, Dionisios Pnevmatikatos, Michail Flouris and Manolis Katevenis, ``Web-Conscious Storage Management for Web Proxies,'' *IEEE Transactions On Networking (TON)*, Vol. 10, No 6, December 2002.

[J6] Dionisios Pnevmatikatos, Ioannis Sourdis and Kyriakos Vlachos, ``An Efficient and Low-Cost Input/Output Subsystem for Network Processors'', *IEEE Design and Test of Computers,* Vol. 20, no. 4, pp. 56-64, July 2003.

[J7] Ioannis Papaefstathiou, Stylianos Perissakis, Theofanis G. Orphanoudakis, Nikos A. Nikolaou, George Kornaros, Nicholas A. Zervos, George Konstantoulakis, Dionisios N. Pnevmatikatos, and Kyriakos Vlachos, ``PRO3: A Hybrid NPU Architecture'', IEEE Micro, Vol. 24, no. 5, pp. 20-33, September/October 2004.

[J8] Koen De Bosschere, Wayne Luk, Xavier Martorell, Nacho Navarro, Michael F. P. O'Boyle, Dionisios N. Pnevmatikatos, Alex Ramírez, Pascal Sainrat, André Seznec, Per Stenström, Olivier Temam: High-Performance Embedded Architecture and Compilation Roadmap. Trans. HiPEAC 1: 5-29 (2007)

[J9] Kyriakos Vlachos, Theofanis Orphanoudakis, Yannis Papaeftathiou, Nikolaos Nikolaou, Dionisios Pnevmatikatos, George Konstantoulakis, J. A. Sanchez-P., ``Design and performance evaluation of a Programmable Packet Processing Engine (PPE) suitable for high-speed network processors units'', Journal of Microprocessors and Microsystems, vol. 31, no 3, 2007.

[J10] Ioannis Sourdis, Dionisios N. Pnevmatikatos, Stamatis Vassiliadis, ``Scalable multigigabit pattern matching for packet inspection'', IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 16 , Issue 2 (February 2008).

[J11] Manolis Katevenis, Vassilis Papaefstathiou, Stamatis G. Kavadias, Dionisios N. Pnevmatikatos, Federico Silla, Dimitrios S. Nikolopoulos, ``Explicit Communication and Synchronization in SARC''. IEEE Micro, vol 30, no 5, pp. 30-41, 2010.

[J12] G Passas, M Katevenis, D Pnevmatikatos, ``Crossbar NoCs Are Scalable Beyond 100 Nodes'', *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 31, no. 4, April 2012.

[J13] George Kornaros, Dionisios N. Pnevmatikatos, ``A survey and taxonomy of on-chip monitoring of multicore systems-on-chip'', ACM Transactions on Design Automation of Electronic Systems 18(2): 17 (2013).

[J14] Ioannis Sourdis, Christos Strydis, A. Armato, Christos-Savvas Bouganis, Babak Falsafi, Georgi Nedeltchev Gaydadjiev, Sebastian Isaza, Alirad Malek, R. Mariani, Dionisios N. Pnevmatikatos, Dhiraj K. Pradhan, Gerard K. Rauwerda, Robert M. Seepers, Rishad A. Shafik, Kim Sunesen, Dimitris Theodoropoulos, Stavros Tzilis, Michalis Vavouras: ``DeSyRe: On-demand system reliability'', *Microprocessors and Microsystems - Embedded Hardware Design* 37(8-C): 981-1001, 2013.

[J15] George Kornaros, Dionisios N. Pnevmatikatos: Dynamic Power and Thermal Management of NoC-Based Heterogeneous MPSoCs. TRETS 7(1): 1 (2014).

[J16] Spyros Lyberis, George Kalokerinos, Michalis Lygerakis, Vassilis Papaefstathiou, Iakovos Mavroidis, Manolis Katevenis, Dionisios N. Pnevmatikatos, Dimitrios S. Nikolopoulos: FPGA prototyping of emerging manycore architectures for parallel programming research using Formic boards. Journal of Systems Architecture - Embedded Systems Design 60(6): 481-493 (2014).

[J17] G. Passas, M. Katevenis, D. Pnevmatikatos: "The Combined Input-Output Queued Crossbar Architecture for High-Radix On-Chip Switches", IEEE Micro, vol. 35, no. 6, November-December 2015, pp. 38-47; DOI: 10.1109/MM.2014.56

[J18] Dionisios N. Pnevmatikatos, Kyprianos Papadimitriou, Tobias Becker, Peter Böhm, Andreas Brokalakis, Karel Bruneel, C. Ciobanu, Tom Davidson, Georgi Gaydadjiev, Karel Heyse, Wayne Luk, Xinyu Niu, Ioannis Papaefstathiou, Danilo Pau, Oliver Pell, Christian Pilato, Marco D. Santambrogio, Donatella Sciuto, Dirk Stroobandt, Tod Todman, Elias Vansteenkiste: FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration. Microprocessors and Microsystems - Embedded Hardware Design 39(4-5): 321-338 (2015), June–July 2015. doi:10.1016/j.micpro.2014.09.006

[J19] R. Giorgi, S. Mazumdar, S. Viola, P. Gai, S. Garzarella, B. Morelli, D. Pnevmatikatos, D. Theodoropoulos, C. Alvarez , E. Ayguade, J. Bueno, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, (2016). Modeling Multi-board Communication in the AXIOM Cyber-Physical System. Ada User Journal, 37(4), 228-235.

[J20] Carlos Álvarez, Eduard Ayguadé, Jaume Bosch, Javier Bueno, Artem Cherkashin, Antonio Filgueras, Daniel Jiménez-González, Xavier Martorell, Nacho Navarro, Miquel Vidal, Dimitris Theodoropoulos, Dionisios N. Pnevmatikatos, Davide Catani, David Oro, Carles Fernández, Carlos Segura, Javier Rodríguez Saeta, Javier Hernando, Claudio Scordino, Paolo Gai, Pierluigi Passera: The AXIOM software layers. Microprocessors and Microsystems - Embedded Hardware Design 47: 262-277 (2016)

[J21] Dimitris Theodoropoulos, Somnath Mazumdar, Eduard Ayguadé, Nicola Bettin, Javier Bueno, Sara Ermini, Antonio Filgueras, Daniel Jiménez-González, Carlos Álvarez-Martínez, Xavier Martorell, Francesco Montefoschi, David Oro, Dionisis N. Pnevmatikatos, Antonio Rizzo, Paolo Gai, Stefano Garzarella, Bruno Morelli, Alberto Pomella, Roberto Giorgi, The AXIOM platform for next-generation cyber physical systems. Microprocessors and Microsystems - Embedded Hardware Design 52: 540-555 (July 2017)

[J22] George Charitopoulos, Iosif Koidis, Kyprianos Papadimitriou, Dionisios Pnevmatikatos, Run-time management of systems with partially reconfigurable FPGAs, Integration, the VLSI Journal, Volume 57, March 2017, Pages 34–44. DOI: 10.1016/j.vlsi.2016.11.008

[J23] Mario Drumond, Alexandros Daglis, Nooshin Mirzadeh, Dmitrii Ustiugov, Javier Picorel, Babak Falsafi, Boris Grot, Dionisios N. Pnevmatikatos: Algorithm/Architecture Co-Design for Near-Memory Processing. Operating Systems Review 52(1): 109-122 (2018)

[J24] George Kalokerinos, Vassilis Papaefstathiou, George Nikiforos, Stamatis G. Kavadias, Xiaojun Yang, Dionisios N. Pnevmatikatos, Manolis Katevenis: Prototyping a Configurable Cache/Scratchpad Memory with Virtualized User-Level RDMA Capability. Trans. High Perform. Embed. Archit. Compil. 5: 100-120 (2019)

[J25] Nikolaos Alachiotis, Charalampos Vatsolakis, Grigorios Chrysos, Dionisios N. Pnevmatikatos: RAiSD-X: A Fast and Accurate FPGA System for the Detection of Positive Selection in Thousands of Genomes. TRETS 13(1): 2:1-2:30 (2020)

Conference Publications (Refereed):

[C1] Dionisios N. Pnevmatikatos, Manoj Franklin, and Gurindar S. Sohi, ``Control Flow Prediction for Dynamic ILP Processors,'' *Proceedings of the 26th Annual International Symposium on Microarchitecture (MICRO-26)*, December 1993, IEEE/ACM.

[C2] Dionisios N. Pnevmatikatos and Gurindar S. Sohi, ``Guarded Execution and Branch Prediction in Dynamic ILP Processors,'' *Proceedings of the 21st Annual International Symposium on Computer Architecture (ISCA-21)*, April 1994, IEEE/ACM.

[C3] Todd M. Austin, Dionisios N. Pnevmatikatos, and Gurindar S. Sohi, ``Streamlining Data Cache Access with Fast Address Calculation,'' *Proceedings of the 22nd Annual International Symposium on Computer Architecture (ISCA-22)*, June 1995, IEEE/ACM.

[C4] Georgios Kornaros, Dionisios Pnevmatikatos, Panagiota Vatsolaki, Georgios Kalokerinos, Chara Xanthaki, Dimitrios Mavroidis, Dimitrios Serpanos, and Manolis Katevenis, ``Implementation of ATLAS I: a Single-Chip ATM Switch with Backpressure'', Proceedings of the *Hot Interconnects VI Symposium*, August 1998.

[C5] Dionisios Pnevmatikatos, Georgios Kornaros, G. Kalokerinos, and Chara Xanthaki, ``The Memory Structures of ATLAS I, a High Performance, 16x16 ATM Switch Supporting Backpressure,'' *Proceedings of the 11th Annual 1998 IEEE International ASIC Conference,* September 1998.

[C6] Georgios Kornaros, Dionisios Pnevmatikatos, Dimitrios Mavroidis, Peni Vatsolaki, George Kalokerinos, Chara Xanthaki, Georgios Dimitriadis, ``On Optimizing ATLAS I, A 10 Gbps ATM Switch,'' *Proceedings of the 7-th Hellenic Conference on Informatics,* Ioannina, Greece, August 26-29, 1999, pp. IV.50-IV.60.

[C7] Dionisios Pnevmatikatos and Georgios Kornaros, ``ATLAS II: Optimizing a 10Gbps Single-chip ATM Switch,'' *12th Annual 1999 IEEE International ASIC/SOC Conference,* Washington, DC, USA, September 15-18, 1999, IEEE.

[C8] Evangelos Markatos, Manolis Katevenis, Dionisios Pnevmatikatos and Michail Flouris, ``Secondary Storage Management for Web Proxies,'' *Proceedings of the 2nd USENIX Symposium on Internet Technologies and Systems (USITS '99),* Boulder, CO, USA, October 12-13, 1999, USENIX.

[C9] Apostolos Dollas, Dionisios Pnevmatikatos, Nikolaos Aslanides, Stamatios Kavvadias, Euripides Sotiriades, Sotiris Zogopoulos, Kyprianos Papademetriou, Architecture and Applications of PLATO, a Reconfigurable Active Network Platform, *Proceedings, 9th International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM-2001)*, Rohnert Park, CA, April 30 - May 2, 2001, IEEE.

[C10] Apostolos Dollas, Nikolaos Aslanides, Stamatios Kavvadias, Euripides Sotiriades, Kyprianos Papademetriou, Dionisios N. Pnevmatikatos, Rapid Prototyping of a Reusable 4x4 Active ATM Switch Core with the PCI Pamette, *Proceedings, 12th International IEEE Workshop on Rapid System Prototyping (RSP-2001)*, pp. 17-23, Monterey, CA, June 25-27, 2001, IEEE.

[C11] Andreas Moshovos, Dionisios Pnevmatikatos, Amirali Baniasadi, ``Slice-Processors: An Implementation of Operation-based Prediction'', *Proceedings of the 15th ACM International Conference on Supercomputing (ICS),* Sorrento, Naples, Italy, June, 16 - 21, 2001, ACM.

[C12] Apostolos Dollas, Dionisios Pnevmatikatos, Nikolaos Aslanides, Euripides Sotiriades, Stamatis Kavvadias, Sotiris Zogopoulos, ``Experimental Testing of PLATO, a Reconfigurable Active ATM Network Node'', *Proceedings of the 8th Panhellenic Informatics Conference*, Cyprus, November, 2001.

[C13] K. Vlachos, T. Orphanoudakis, N. Nikolaou, S. Perissakis, D. Pnevmatikatos, G. Kornaros, J.A. Sanchez and G. Konstantoulakis, ``Processing and Scheduling Components in an Innovative Network Processor Architecture'', *Proceedings of the International Conference on VLSI Design,* New Dehli, India, January 4-8, 2003. (7 pages) IEEE, ACM.

[C14] Ioannis Sourdis Dionisios Pnevmatikatos, and Kyriakos Vlachos, ``An Efficient and Low-Cost Input/Output Subsystem for Network Processors'', *Workshop on Application Specific Processors (WASP-1),* November 19, 2002, Istanbul, Turkey (8 pages).

[C15] George Lykakis, Nikolaos Mouratidis, George Konstantoulakis, Kyriakos Vlachos, Nikolaos Nikolaou, Stylianos Perissakis, Ioannis Sourdis, Dionisios Pnevmatikatos, Dionisios Reisis, ``Efficient Field Processing Cores In An Innovative Protocol Processor System-On-Chip'', *Design Automation and Test Europe (DATE)*, March 3-7, 2003, Munich, Germany.

[C16] Ioannis Sourdis and Dionisios Pnevmatikatos, ``Fast, Large-Scale String Match for a 10Gbps FPGA-based Network Intrusion Detection System'', *13th International Conference on Field Programmable Logic and Applications (FPL)*, September 1-3, 2003, Lisbon – Portugal. Awarded "Significant paper" of the first 25 years of the FPL conference (one out of 27 total).

[C17] I. Charitakis, Dionisios Pnevmatikatos, Evangelos Markatos, Kostas Anagnostakis ``S2I: a Tool for Automatic Rule Match Compilation for the IXP Network Processor''. Proceedings of the 7th International Workshop on Software and Compilers for Embedded Systems, SCOPES 2003, pp.226-239, September 24-26, 2003 Vienna - Austria.

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