Άσκηση 2

blackscholes (test)

- max ILP (superscalar)

- Πιθανώς αρκετά long-latency events τα οποία γίνονται overlapped με μεγαλύτερο ROB
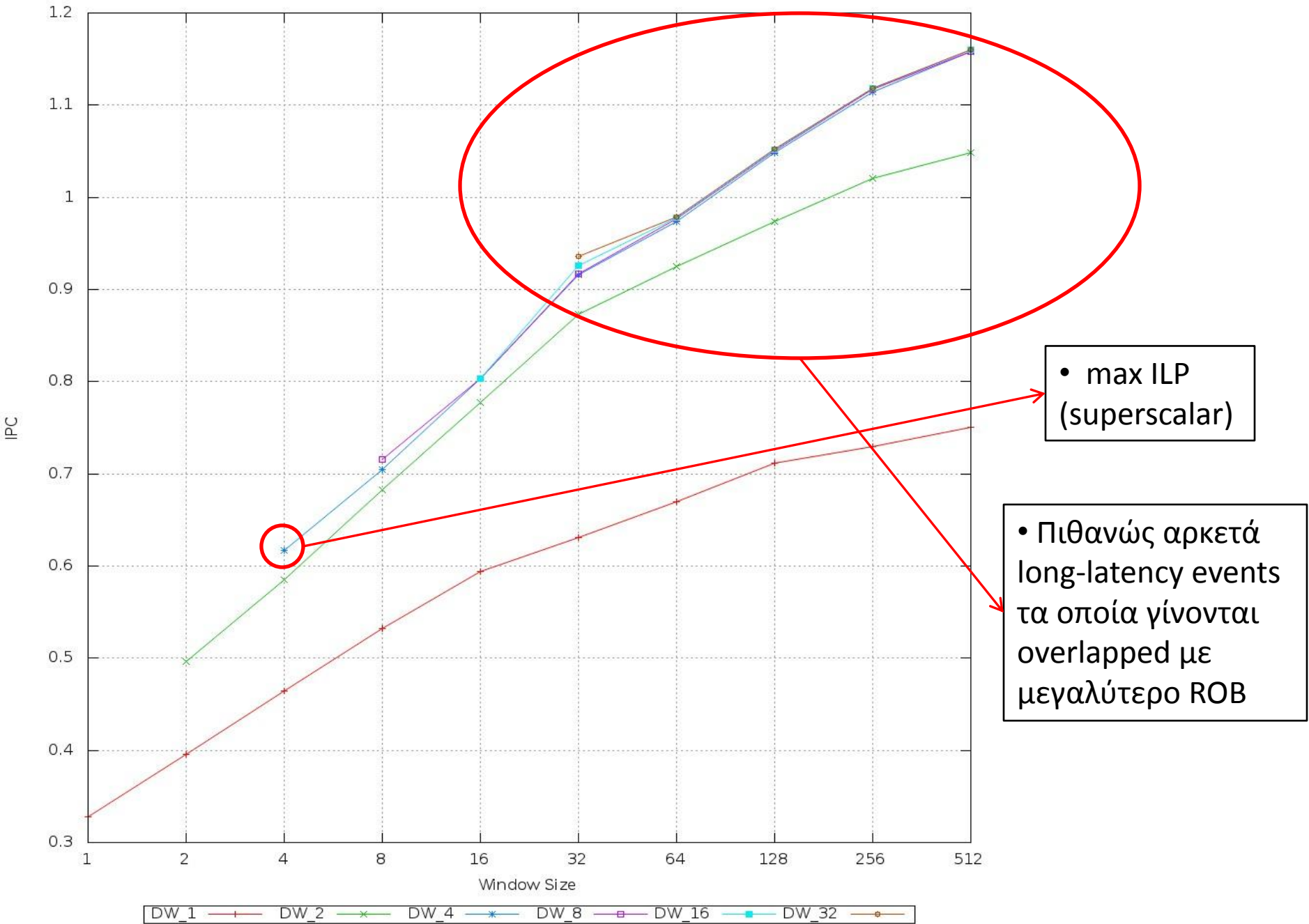
blackscholes (small)

bodytrack (test)

- max ILP (superscalar)

- Περιορισμένος αριθμός ανεξάρτητων εντολών
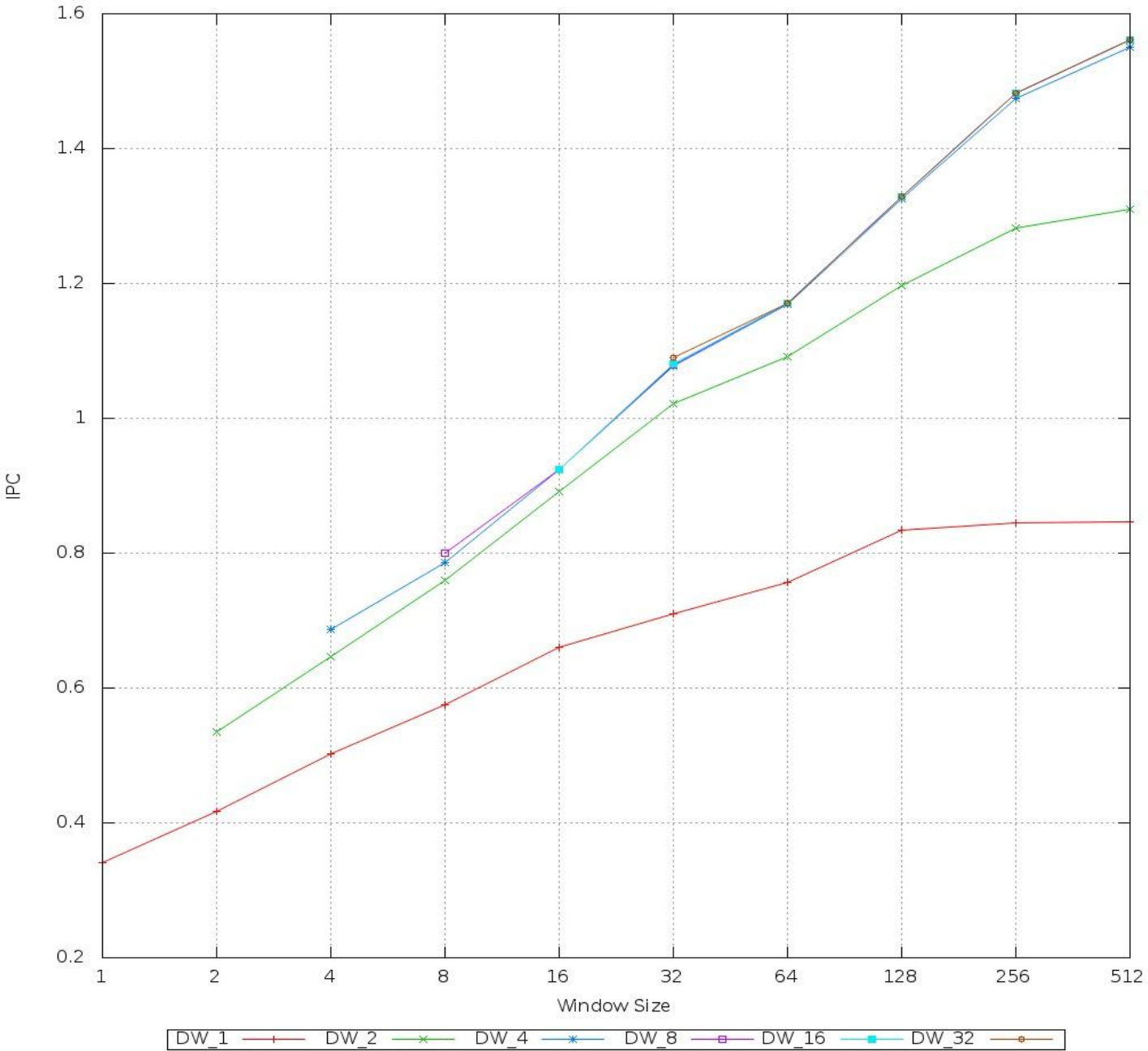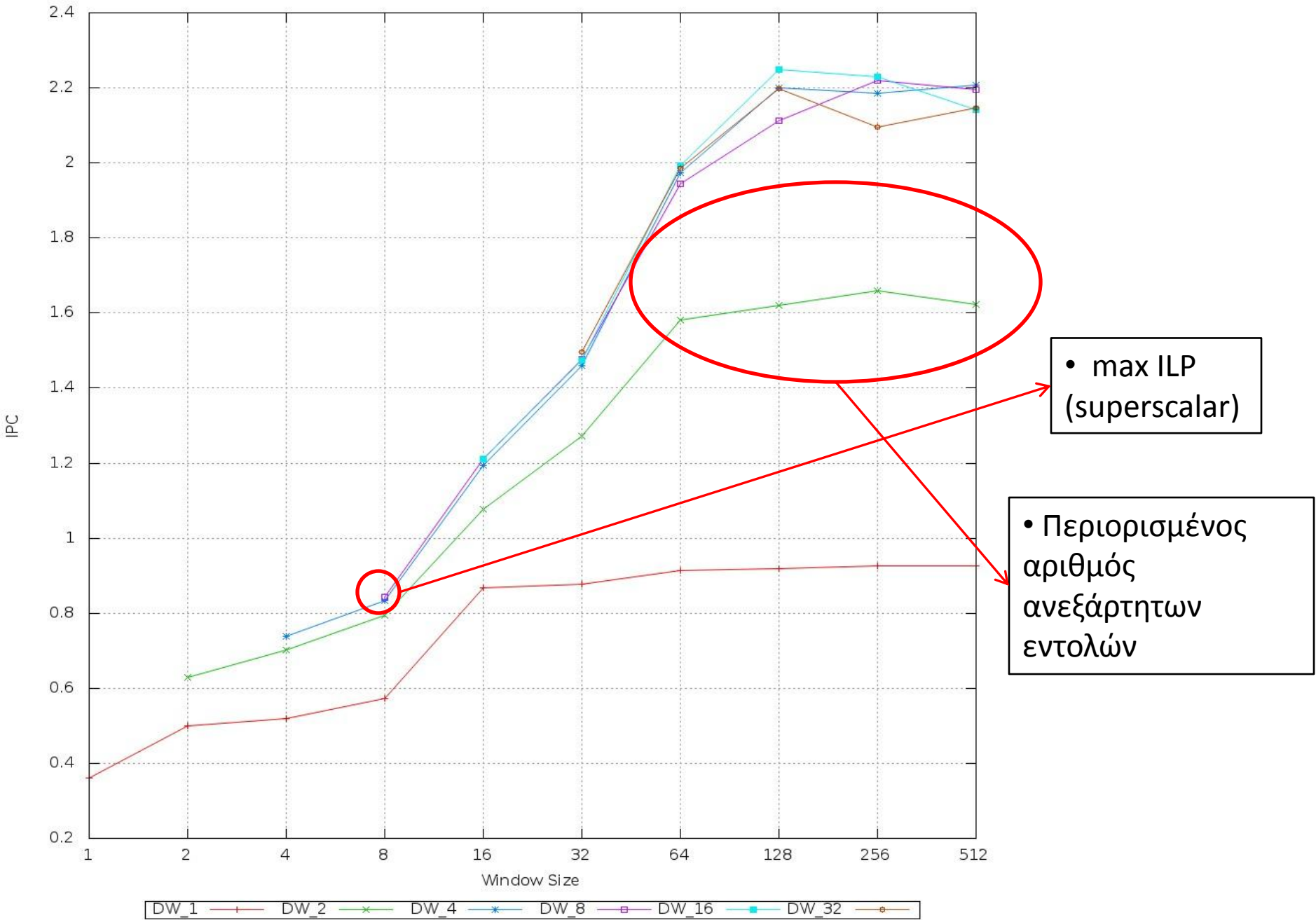
bodytrack (small)

swaptions

IPC vs Window Size

Legend: DW_1, DW_2, DW_4, DW_8, DW_16, DW_32
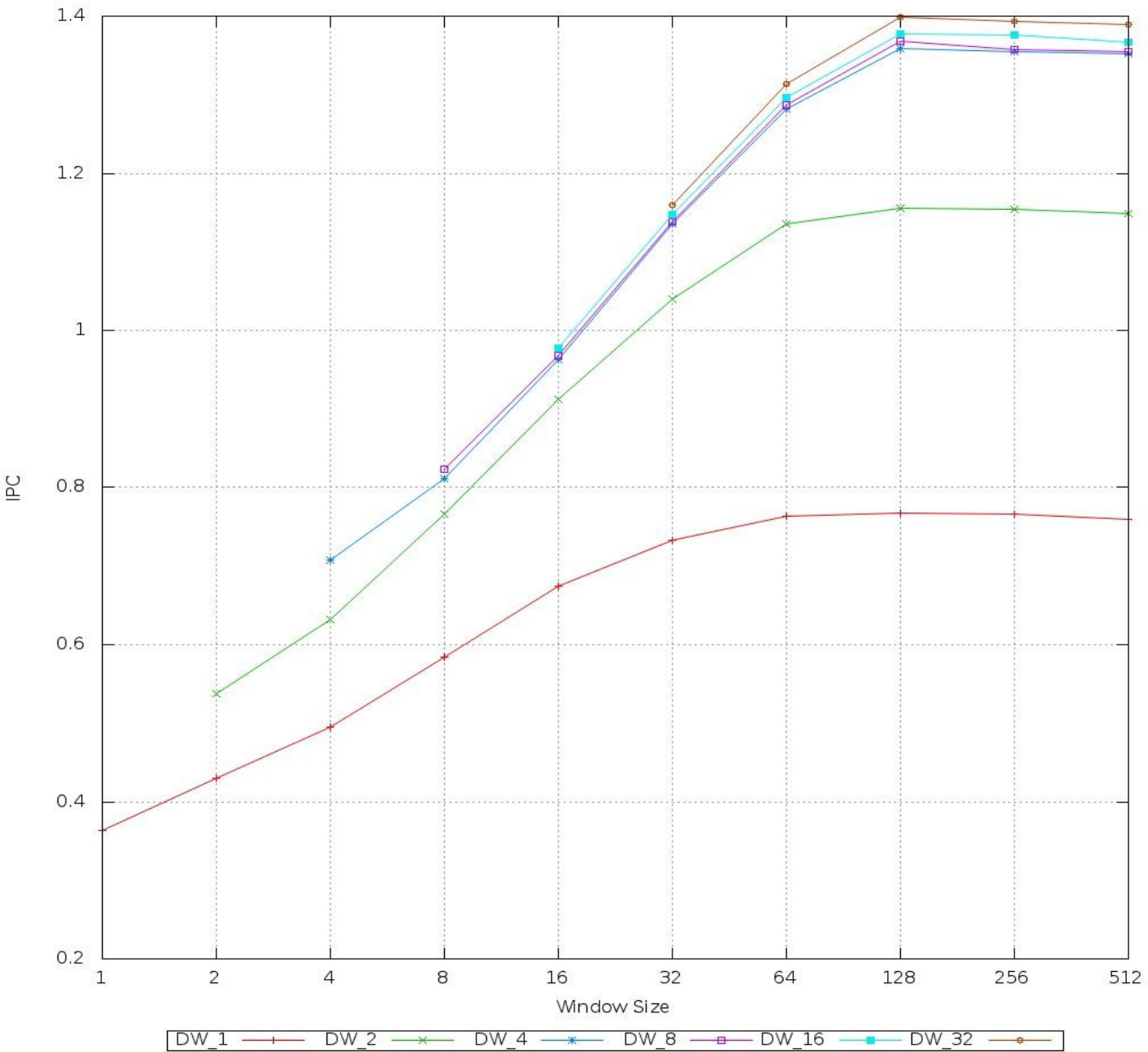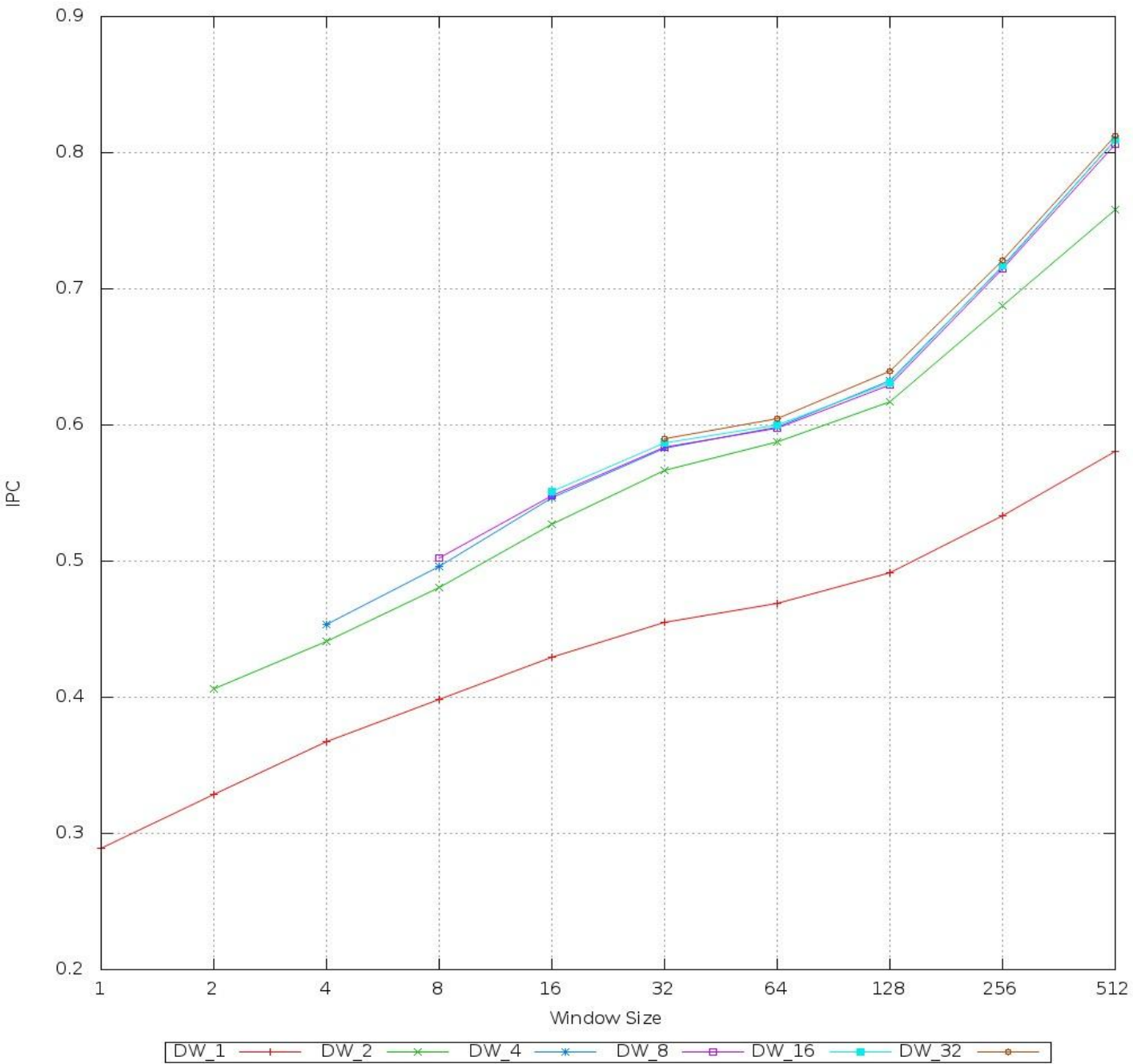
canneal (test)

canneal (small)

dedup (test)

Intel processors

Nehalem (2008) – 45nm
- Dispatch_width = 4
- Window_size = 128

Sandy Bridge (2011) – 32nm
- Dispatch_width = 4
- Window_size = 168

Haswell (2013) – 22nm
- Dispatch_width = 8
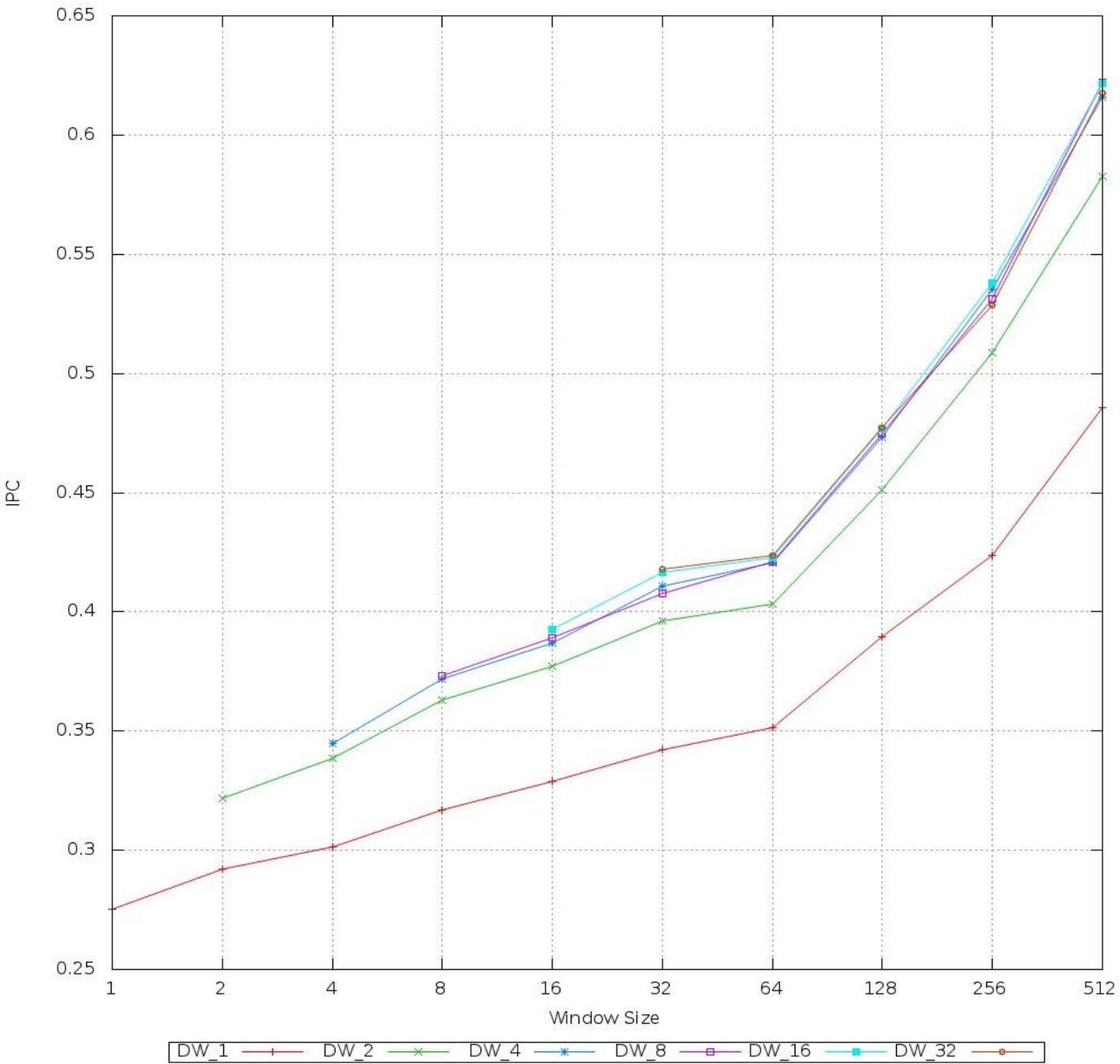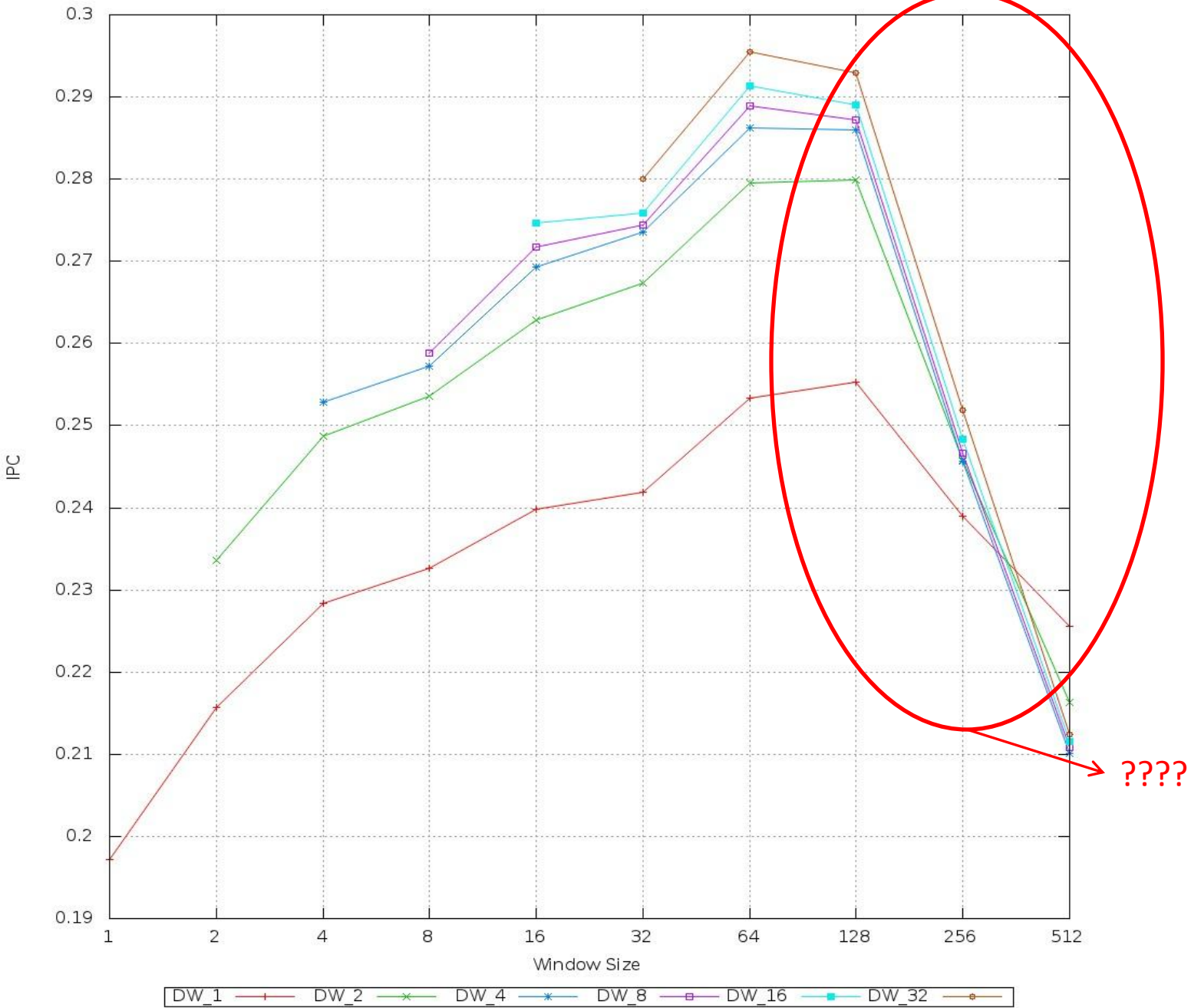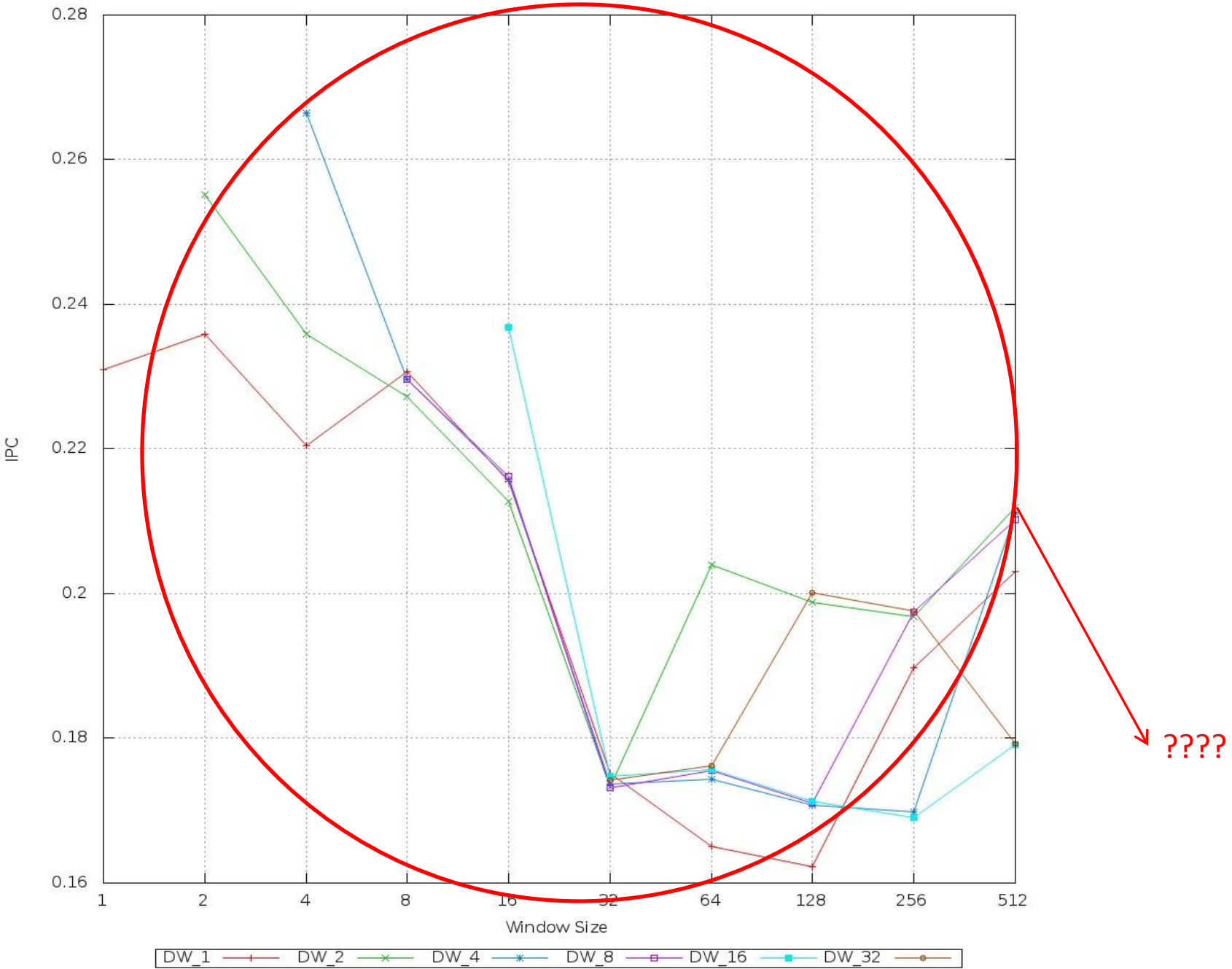- Window_size = 192

Tomasulo

	OP	IS	EX	WR	CMT	Σχόλιο
LD	F0,0(R1)	1	2 - 6	7	8	Miss A[0] → Fetch A[0]A[1] in block0, LRU=1
ADDI	R3, R1, 0x10	2	3	4	9	R3 points to A[2]
LD	F1, 0(R3)	3	5 – 9	10	11	Miss A[2] → Fetch A[2]A[3] in block1, LRU=0
ADDD	F0, F0, F1	4	11	12	13	
DIVD	F0,F0, 0x2	5	13 - 17	18	19	
SD	F0, 0(R2)	6	19	20	21	Hit A[0] → LRU=1
ADDI	R2, R2, 0x8	7	8	9	22	R2 points to A[1]
ADDI	R1, R1, 0x18	9	10	11	23	R1 points to A[3]
SUBI	R8, R8, 0x1	10	11	13	24	CDB conflict, R8 = 1
BNEZ	R8, LOOP	12	14	15	25	pred = T, res = T, new value = 11
LD	F0,0(R1)	14	15	16	26	Hit A[3] → LRU=0
ADDI	R3, R1, 0x10	20	21	22	27	R3 points to A[5]
LD	F1, 0(R3)	22	23 - 27	28	29	Miss A[5] → Fetch A[4]A[5] in block0, LRU=1
ADDD	F0, F0, F1	23	29	30	31	
DIVD	F0,F0, 0x2	24	31 - 35	36	37	
SD	F0, 0(R2)	25	37 - 41	42	43	Miss A[1] → Fetch A[0]A[1] in block1, LRU=0
ADDI	R2, R2, 0x8	26	27	29	44	R2 points to A[2]
ADDI	R1, R1, 0x18	27	28	31	45	CDB conflict, R1 points to A[6]
SUBI	R8, R8, 0x1	28	29	32	46	CDB conflict, R8 = 0
BNEZ	R8, LOOP	30	33	34	47	pred = T, res = NT, new value = 10
LD	F1, 0(R3)	32	33 -			Miss A[6] → Fetch A[6]A[7] in block 0, LRU = 1, FLUSH @ 34
ADDI	R3, R2, 0x10	35	36	37	48	R3 points to A[4]
LD	F0, 0(R3)	38	39 - 43	44	49	Miss A[4] → Fetch A[4]A[5] in block 1, LRU = 0
ADDI	R4, R2, 0x8	44	45	46	50	R4 points to A[3]
LD	F1, 0(R4)	45	47 – 51	52	53	Miss A[3] → Fetch A[2]A[3] in block 0, LRU = 1
SUBD	F0, F0, F1	46	53	54	55	
SD	F0, 0(R2)	47	55	56	57	Hit A[2]